CLAIMS

1. (currently amended) A clock generator, comprising:

(a) a phase detector;

(b) a counter;

(c) clock-generation circuitry; and

(d) a programmable lock detection and correction (PLDC) circuit, wherein:

the clock-generation circuitry is adapted to generate a plurality of clock signals having different relative phases based on a count value received from the counter;

the counter is adapted to accumulate digital control signals received from the phase detector in order to generate the count value;

the phase detector is adapted to compare a reference clock signal to a feedback signal derived from one of the clock signals generated by the clock-generation circuitry in order to generate the digital control signals for the counter;

the PLDC circuit receives an input control signal specifying one of a plurality of different possible input control values, each input control value corresponding to one of a plurality of different possible programmable accuracy levels; and

the PLDC circuit is adapted to determine (1) whether operations of the clock generator have settled to a stable operating point to within [[a]] the programmable accuracy level corresponding to the input control value specified by the input control signal and (2) whether the stable operating point corresponds to a proper lock state for the clock generator.

2. (original) The invention of claim 1, wherein:

the clock-generation circuitry is a digitally controlled, multiple-tap delay line; and

the phase detector, counter, and clock-generation circuitry form a delay-locked loop.

3. (currently amended) The invention of claim 1, wherein the PLDC circuit comprises:

a count check circuit adapted to compare the difference between count values over a specified time period to [[an]] the input control value corresponding to the ~~user-programmable~~ programmable accuracy level to determine whether or not the operations of the clock generator have settled to a stable operating point; and

a phase check circuit adapted to compare the reference clock to the two or more clock signals from the clock-generation circuitry to determine whether or not the stable operating point corresponds to a proper lock state for the clock generator.

4. (original) The invention of claim 3, wherein the specified time period is programmable and the count value is based on a counter step size that is programmable.

5. (original) The invention of claim 3, wherein the phase check circuit performs its operations only after the count check circuit has determined that the operations of the clock generator have settled to a stable operating point.

6. (original) The invention of claim 3, wherein the count check circuit compares the count value at two or more instances during the specified period to compute difference values, wherein when substantially all difference values are less than or equal to the control value for the comparisons during the specified period, an enable signal is asserted toward the phase check circuit, the signal indicating to the phase check circuit that the operations of the clock generator have settled to a stable operating point.

7. (original) The invention of claim 3, wherein the phase check circuit includes:

a first block of combinatorial logic adapted to determine the state of a LOCKED output signal from a first flip-flop based on a first Boolean function of the two or more clock signals, wherein when the waveform relationships of the two or more clock signals indicate that the feedback signal is of substantially the same period as the reference clock, LOCKED is asserted TRUE;

a second block of combinatorial logic adapted to determine the state of a LOOPRESET output signal from a second flip-flop based on a second Boolean function of the two or more clock signals, wherein when the waveform relationships of the two or more clock signals indicate that the feedback signal is not of substantially the same period as the reference clock, LOOPRESET is asserted TRUE; and

a third block of combinatorial logic adapted to determine a clear signal for the first and second flip-flops based on a third Boolean function of an enable signal and a reset signal.

8. (original) The invention of claim 1, wherein the PLDC generates a control signal that causes the counter to reset the count value when the PLDC determines that the stable operating point corresponds to an improper lock state for the clock generator.

9. (currently amended) A programmable lock detection and correction (PLDC) circuit for a multiphase clock generator (MCG), the PLDC circuit comprising:

circuitry that receives an input control signal specifying one of a plurality of different possible input control values, each input control value corresponding to one of a plurality of different possible programmable accuracy levels;

circuitry adapted to determine whether operations of the MCG have settled to a stable operating point to within [[a]] the programmable accuracy level corresponding to the input control value specified by the input control signal; and

circuitry adapted to determine whether the stable operating point corresponds to a proper lock state for the MCG.

10. (original) The invention of claim 9, wherein the MCG comprises a phase detector; a counter; and clock-generation circuitry, wherein:

the clock-generation circuitry is adapted to generate a plurality of clock signals having different relative phases based on a count value received from the counter;

the counter is adapted to accumulate digital control signals received from the phase detector in order to generate the count value;

the phase detector is adapted to compare a reference clock signal to a feedback signal derived from one of the clock signals generated by the clock-generation circuitry in order to generate the digital control signals for the counter.

11. (original) The invention of claim 10, wherein:

the clock-generation circuitry is a digitally controlled, multiple-tap delay line; and

the phase detector, counter, and clock-generation circuitry form a delay-locked loop.

12. (currently amended) The invention of claim 10, wherein the PLDC circuit comprises:

a count check circuit adapted to compare the difference between count values over a specified time period to [[an]] the input control value corresponding to the ~~user-programmable~~ programmable accuracy level to determine whether or not the operations of the clock generator have settled to a stable operating point; and

a phase check circuit adapted to compare the reference clock to the two or more clock signals from the clock-generation circuitry to determine whether or not the stable operating point corresponds to a proper lock state for the clock generator.

13. (original) The invention of claim 12, wherein the specified time period is programmable.

14. (original) The invention of claim 13, wherein the count value is based on a counter step size that is programmable.

15. (original) The invention of claim 12, wherein the phase check circuit performs its operations only after the count check circuit has determined that the operations of the clock generator have settled to a stable operating point.

16. (original) The invention of claim 12, wherein the count check circuit compares the count value at two or more instances during the specified period to compute difference values, wherein when substantially all difference values are less than or equal to the control value for the comparisons during the specified period, an enable signal is asserted toward the phase check circuit, the signal indicating to the phase check circuit that the operations of the clock generator have settled to a stable operating point.

17. (original) The invention of claim 12, wherein the phase check circuit includes:

a first block of combinatorial logic adapted to determine the state of a LOCKED output signal from a first flip-flop based on a first Boolean function of the two or more clock signals, wherein when the waveform relationships of the two or more clock signals indicate that the feedback signal is of substantially the same period as the reference clock, LOCKED is asserted TRUE;

a second block of combinatorial logic adapted to determine the state of a LOOPRESET output signal from a second flip-flop based on a second Boolean function of the two or more clock signals, wherein when the waveform relationships of the two or more clock signals indicate that the feedback signal is not of substantially the same period as the reference clock, LOOPRESET is asserted TRUE; and

a third block of combinatorial logic adapted to determine a clear signal for the first and second flip-flops based on a third Boolean function of an enable signal and a reset signal.

18. (currently amended) The invention of claim [[12]] 10, wherein the PLDC generates a control signal that causes the counter to reset the count value when the PLDC determines that the stable operating point corresponds to an improper lock state for the clock generator.

19. (currently amended) A method for monitoring operations of a multiphase clock generator (MCG), comprising:

receiving an input control signal specifying one of a plurality of different possible input control values, each input control value corresponding to one of a plurality of different possible programmable accuracy levels;

determining whether operations of the MCG have settled to a stable operating point to within [[a]] the programmable accuracy level corresponding to the input control value specified by the input control signal; and

determining whether the stable operating point corresponds to a proper lock state for the MCG.

20. (currently amended) The invention of claim 19, wherein the MCG comprises:

(a) a phase detector;

(b) a counter;

(c) clock-generation circuitry; and

(d) a programmable lock detection and correction (PLDC) circuit, wherein:

the clock-generation circuitry is adapted to generate at least one output clock signal having a relative phase based on a count value received from the counter;

the counter is adapted to accumulate digital control signals received from the phase detector in order to generate the count value;

the phase detector is adapted to compare a reference clock signal to a feedback signal output from the clock-generation circuitry in order to generate the digital control signals for the counter; and

the PLDC circuit is adapted to determine (1) whether operations of the clock generator have settled to a stable operating point to within [[a]] the programmable accuracy level and (2) whether the stable operating point corresponds to a proper lock state for the clock generator, wherein the determining involves comparing the count to a lower and upper count bound and resetting the counter to a starting count value if the count is less than the lower count bound or is greater than the upper count bound.

21. (original) A programmable lock detection and correction (PLDC) circuit for a multiphase clock generator (MCG), the PLDC circuit comprising:

a count check circuit adapted to compare a difference between count values within the MCG to an input control value corresponding to a user-programmable accuracy level to determine whether the MCG has settled to a stable operating point; and

a phase check circuit adapted to compare a reference clock for the MCG to two or more clock signals generated by the MCG to determine whether the stable operating point corresponds to a proper lock state for the MCG.